IN THE DRAWINGS

Please amend FIGS. 2B, 5B, 7 and 9, as indicated on the attached marked-up copy of original FIGS. 2B, 5B, 7 and 9, to include the label "prior art." No new matter is introduced.

REMARKS

The present application was filed on January 5, 2004 with claims 1 through 42. Claims 1 through 42 are presently pending in the above-identified patent application. Claims 38-42 are proposed to be cancelled herein, without prejudice.

In the Office Action, the Examiner has made a prior restriction requirement final. The Examiner has objected to the Specification for not disclosing the subject matter recited in claim 32. The Examiner has requested that a prior art label be added to Figures 1B, 2B, 4B, 5B, and 6-9. The Examiner has objected to the formal drawings, and requested that they be labeled as "Replacement Sheets." With regard to claim 22, the Examiner asserts that the Drawings do not show an electrical connection between the control line and signal line. Claims 1-2, 9-10, 13-15, 21, 23, 31 and 35 were rejected under 35 USC 102(b) as being anticipated by Mead et al. (United States Patent No. 5,844,265). The Examiner objected to claims 3-8, 11-12, 16-20, 22, 24-30, 32-34 and 36-37 as being dependent on a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Restriction Requirement

The Examiner has made a prior restriction requirement final. Applicants have canceled the unelected claims, 38-42, without prejudice.

Formal Objections

Claim 32

The Examiner has objected to the Specification for not disclosing the subject matter recited in claim 32. To the extent that Applicant understands the Examiner's concerns with regard to Claim 32, Applicant notes that Claim 32 is directed to a basic method of operation of the gated diode amplifier, and how to modify the voltage of the control line. Claim 32 requires that the gated diode further comprises an n-type gated diode, wherein the threshold voltage is a positive voltage and wherein the step of modifying voltage on a control line comprises the step of raising voltage from about ground to a predetermined positive voltage.

For an n-type gated diode, the first terminal is the gate (Claim 21) and the second terminal is the source (Claim 21). Applicant submits that Figures 11A, 11B, 11C, 12A, 12B and Fig. 14, and the associated text in the description illustrate the configuration of claim 32, when the

threshold voltage of the gated diode is a positive voltage, and the voltage on the control line (i.e., Vs) is raised from about ground to a predetermined positive voltage (say VB).

Drawings

The Examiner has requested that a prior art label be added to Figures 1B, 2B, 4B, 5B, and 6-9. The Examiner has objected to the formal drawings, and requested that they be labeled as "Replacement Sheets." Applicant submits that Figs. 1A, 1B, 1C, 4A, 4B, 6 and 8 show a gated diode structure with only a gate and a source (and no drain). There are only two terminal areas for the gated diode. The present invention recognizes that this structure without the drain leads to significantly smaller gated diode physical structure (which keeps the area much smaller in applications such as memories and sense amplifiers). Thus, Figs. 1A, 1B, 1C, 4A, 4B, 6 and 8 are different from what is shown by the prior art, including Mead.

Applicants have labeled Figures 2B, 5B, 7 and 9 as "prior art" in accordance with the Examiner's suggestion and each sheet has been labeled as a "Replacement Sheet."

Applicants respectfully request entry of the amendment to FIGS. 2B, 5B, 7 and 9, as indicated on the attached marked-up copy of original FIGS. 2B, 5B, 7 and 9 submitted herewith for the Examiner's approval, and request the that the objection to the drawings be withdrawn. No new matter has been introduced.

Claim 22

With regard to claim 22, the Examiner asserts that the Drawings do not show an electrical connection between the control line and signal line. Applicant submits that the configuration of claim 22 does not require an electrical connection between the control line and signal line.

Claim 22 is directed to a basic method of operation of the gated diode amplifier, and how to modify the voltage of the control line. Claim 22 requires that a sensed voltage is determined based on a voltage at the output, whereby the sensed voltage will be amplified when a voltage on the first terminal relative to the second terminal is above the threshold voltage and will not be amplified when a voltage on the first terminal relative to the second terminal is below the threshold voltage. Support for Claim 22 can be found in the original specification, for example, in Figs. 11A, 11B, 11C, 12A, 12B, 14 and 16 and the corresponding text.

As the Examiner has pointed out, the sensed voltage is necessarily the same as the voltage on the signal line.

For an n-type gated diode, the first terminal is the gate (Claim 21), the second terminal is the source (Claim 21), so the "voltage of the first terminal relative to the second terminal" is Vgs.

If Vgs > Vthreshold (or Vt or Vt_gd as denoted in the description), the gated diode stores charges in the inversion layer and has a large capacitance Cgs; when the voltage Vs of the second terminal (i.e., the source coupled to the control line) is modified (as required by Claim 21) (by raising from low to high, say VB), the voltage at the first terminal (Vg) will be raised to Vout(1) = VB*Rc/(1+Rc)+VL_HIGH, as shown also in Figure 12A. {Signal Amplification}

If Vgs < Vthreshold (or Vt or Vt_gd as denoted in the description), the gated diode stores very little charge and has a very small capacitance Cgs; when the voltage Vs of the second terminal (i.e., the source coupled to the control line) is modified (as required by Claim 21) (by raising from low to high, say VB), the voltage at the first terminal (Vg) will be raised only slightly to Vout(0) = VB*rc/(1+rc)+VL_LOW, as shown in Figure 12A. {No Signal Amplification}

Here, Rc and rc as defined in the description, Rc >> rc (e.g., Rc = 10, rc = 0.1), dVin = VL_HIGH - VL_LOW (typically VL_LOW ~ 0). The difference between the two cases determines the gain of the signal amplification. Gain = (Vout(1) - Vout(0)) / (VB_HIGH - 0), is typically greater than 1.

Thus, Applicant respectfully requests withdrawal of the formal objections.

Prior Art Rejections

Claims 1-2, 9-10, 13-15, 21, 23, 31 and 35 were rejected under 35 USC 102(b) as being anticipated by Mead et al. (United States Patent No. 5,844,265). The Examiner asserts that:

> Mead discloses a circuit 10 for amplifying signals. The circuit 10 comprises a control line (LOAD BIAS connected to a bias voltage source); and
>
> a two terminal semiconductor device 62-1 (MOS transistor used as varactor with source and drain short-circuited), having first and second terminals, the first terminal (gate of varactor 62-2) coupled to a signal line 194-1 (of sense amplifier 10), and the second terminal coupled to the control line (capacitively, through 16-1), where the two terminal semiconductor device is adapted ....

Office Action, par. 5 (internal citations omitted).

Initially, it is noted that the varactors (62-n) of Mead are not even used for signal amplification. Rather, "(u)se of a varactor structure allows compression of the output signal over a wide dynamic range of input signals." See, Col. 3, lines 25 – 26. The Examiner is asserting that the *three* terminal MOS transistors 62-1 through 62-4 in FIG. 7 of Mead are two terminal devices, because the source and drain of the transistors 62-n are short circuited. *Assuming* for the sake of argument that the transistors 62-1 through 62-4 with connected source and drain are two terminal devices, Mead still does not teach at least one a number of other limitations of the independent claims. The present invention does not claim a two-terminal structure by itself. Rather, each independent claim explicitly recites connecting such two-terminal devices in a certain way to perform signal amplification.

The transistors 62-n of FIG. 7, such as transistor 62-1, are connected between a LOAD BIAS (the Examiner is calling this the control line) and first sense line 194-1 (the Examiner is calling this the signal line).

First, the transistors 62-n in Fig. 7 are not directly connected to the LOAD BIAS, but rather are connected to the LOAD BIAS via the output signal (not numbered in FIG. 7 of Mead, but numbered as OUT or 28 in FIG. 1 of Mead). It is noted that the LOAD BIAS is a DC voltage to bias the amplifier which comprises the transistors 12, 14 and 16 in FIG. 1 (often referred to as a cascode amplifer).

Both independent claims 1 and 21 require that "the second terminal (is) ***coupled*** to the control line." Assuming, for the sake of argument, that one even considers the LOAD BIAS as a control line, the varactors (62-n) are not ***coupled*** to a control line. Indeed, it is coupled or directly connected to the output of the amplifier which is clearly a signal, numbered as OUT or 28 in FIG. 1 of Mead). Further, in Column 3, lines 23 - 25 of Mead, it is noted that "... a varactor may be connected between the input and output of amplifier." The input and output of an amplifier are signals, which **cannot** be considered as a control line.

Thus, Mead does not disclose or suggest that "the second terminal (is) ***coupled*** to the control line," as required by independent claims 1 and 21.

Applicants respectfully request that the rejection under section 102 be withdrawn.

Dependent Claims

The Examiner has already indicated that claims 3-8, 11-12, 16-20, 22, 24-30, 32-34 and 36-37 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The remaining dependent claims are dependent on independent claims 1 and 21, and are therefore patentably distinguished over Mead because of their dependency from independent claims 1 and 21 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims following entry of the amendments, i.e., claims 1-37, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

Date: December 13, 2005

Kevin M. Mason
Attorney for Applicants
Reg. No. 36,597
Ryan, Mason & Lewis, LLP
1300 Post Road, Suite 205
Fairfield, CT 06824
(203) 255-6560

ANNOTATED

FIG. 2A

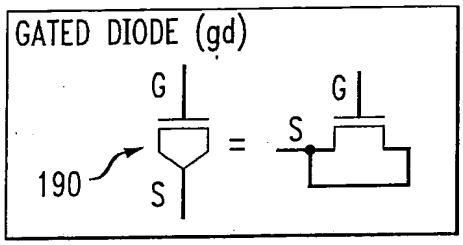

FIG. 2B
Prior Art

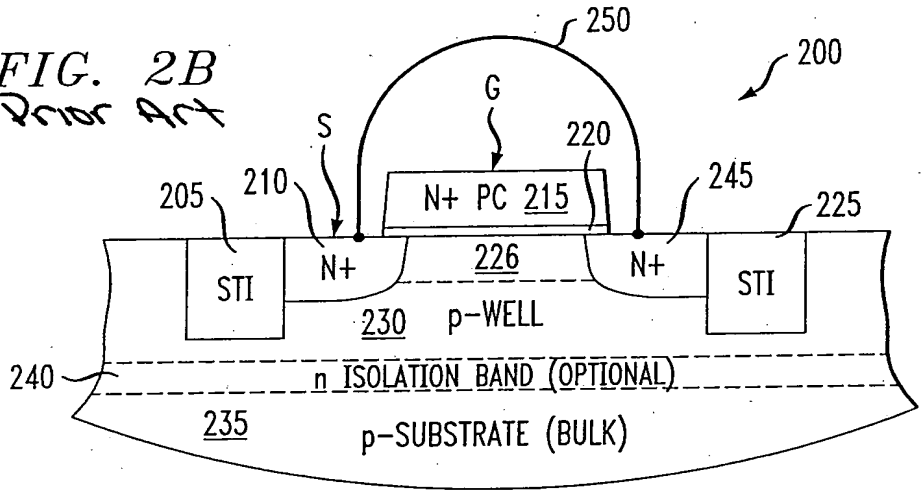

FIG. 2C

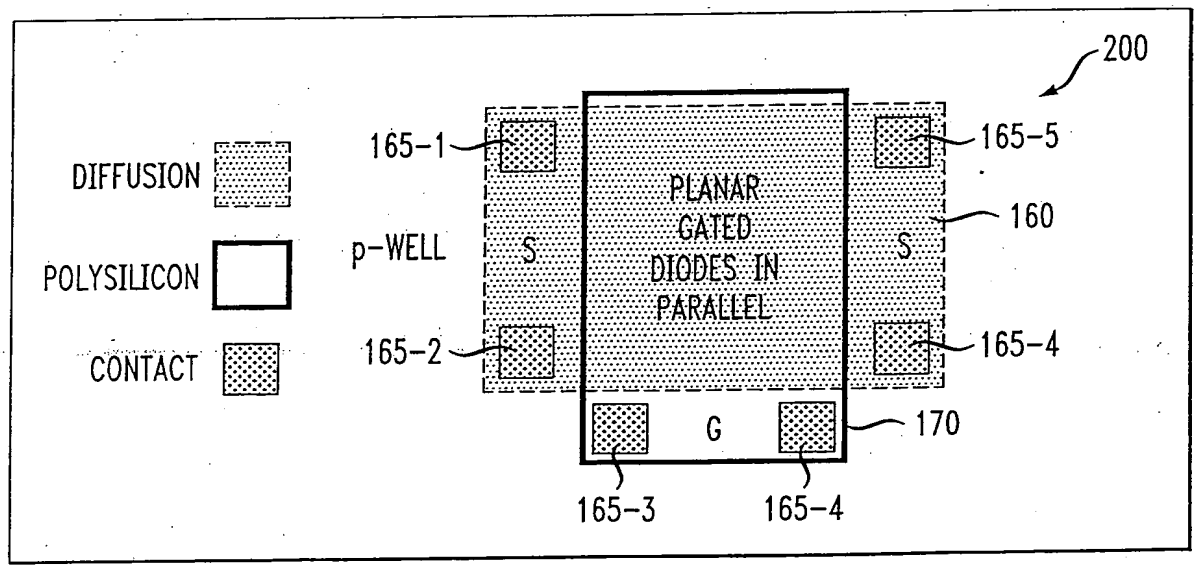

FIG. 5A

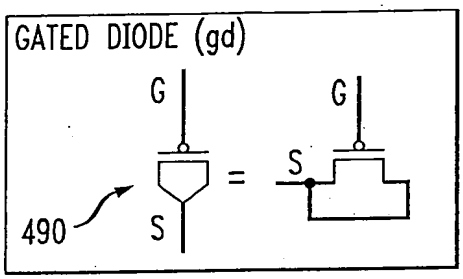

FIG. 5B
Prior Art

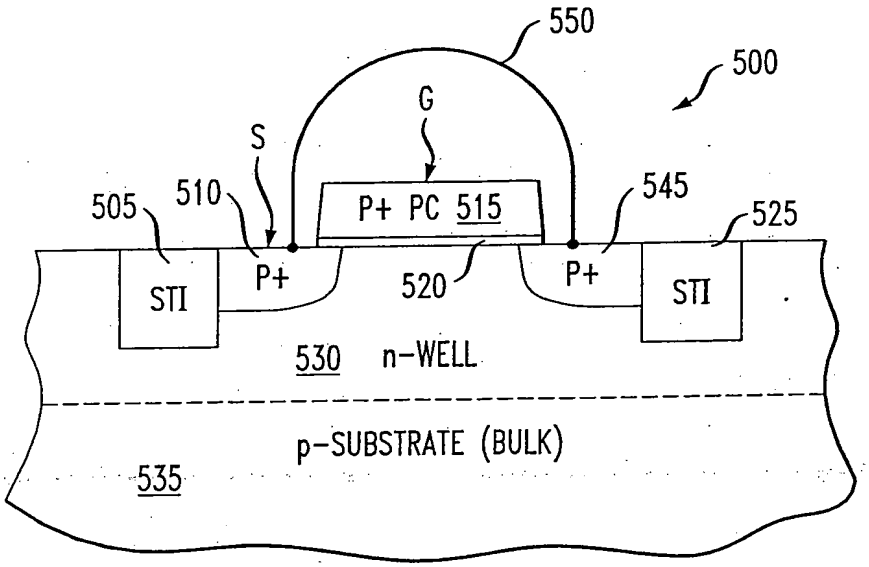

FIG. 6

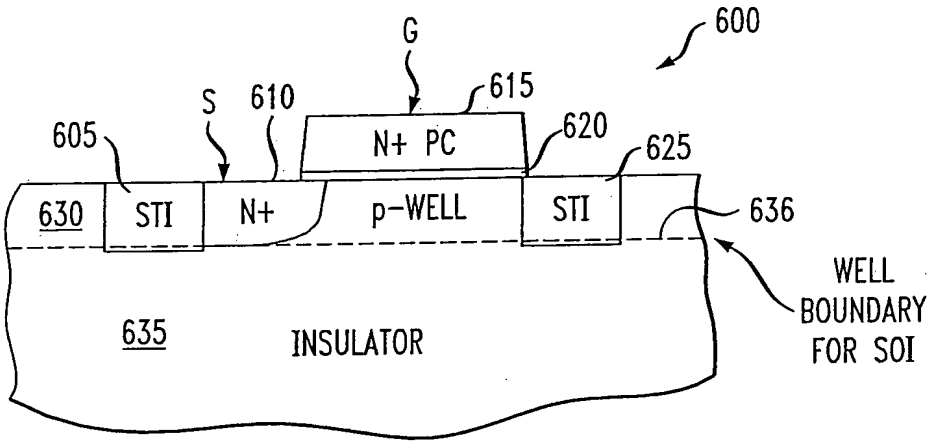

FIG. 7
Prior Art

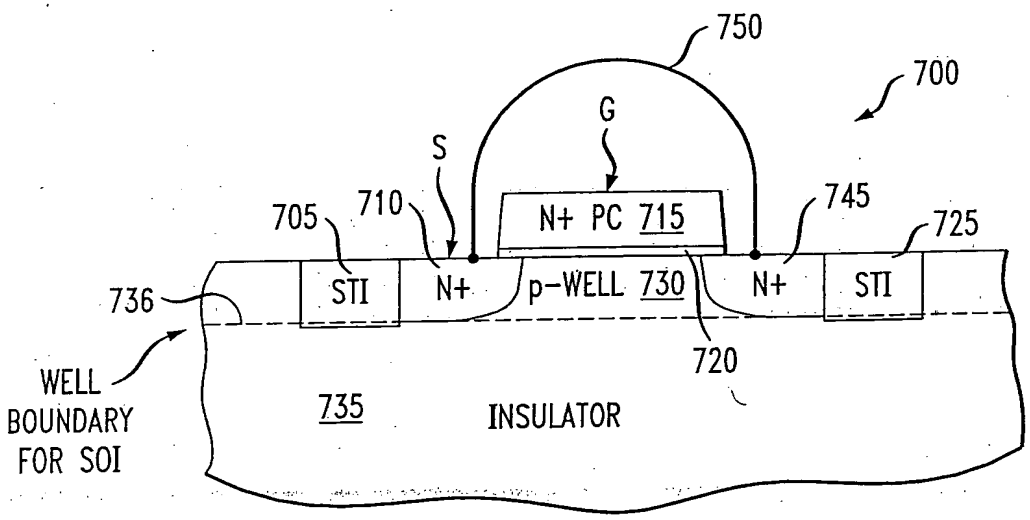

FIG. 8

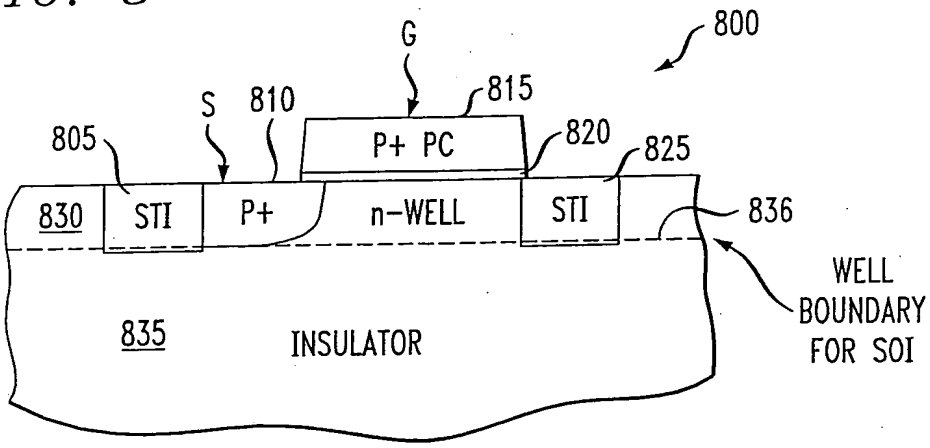

FIG. 9
Prior Art

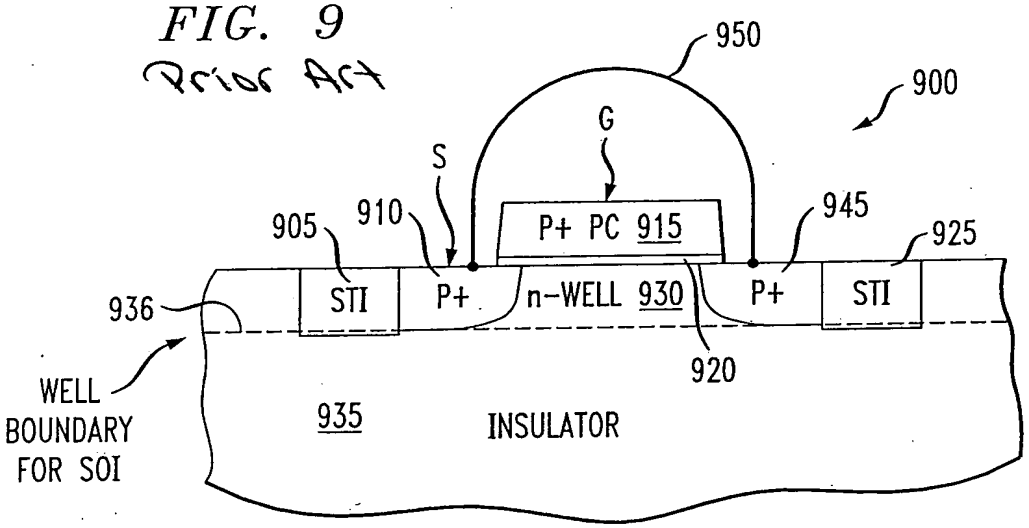

FIG. 10

LINEAR CAPACITOR
GAIN = dVout/dVin = 1